NEC
NEC Electronics Inc.

μPD80C42 8-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH UNIVERSAL PPI

Description

The μPD80C42 is a CMOS programmable peripheral interface controller which contains its own 8-bit microcomputer. It is well suited for use in master/slave configurations or as an intelligent peripheral device in applications requiring very low power consumption. The μPD80C42 has a CPU, 2K bytes of RAM, and 8-bit timer/counter, and I/O ports. I/O capability can be expanded by adding a μPD82C43, which interfaces directly to the μPD80C42. The external bus structure and associated control signals allow easy interfacing to 8048, 8085, and other microprocessor systems. The two standby modes allow even further reduction of power consumption in energy conscious systems.

With the exception of the $\overline{\text{STOP}}$ pin, the μPD80C42 is pin-for-pin compatible with the μPD8041A and the μPD8741A.

Features

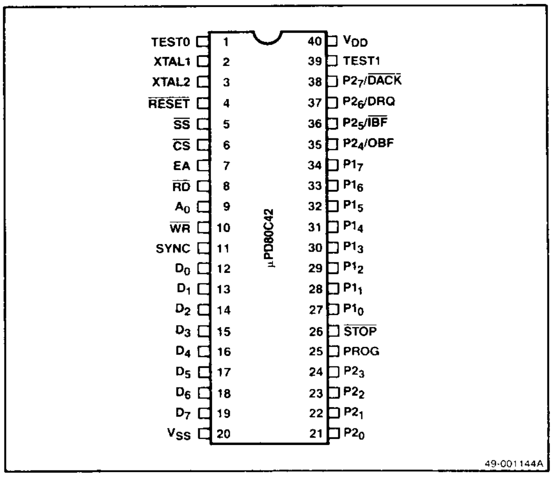
- CMOS technology
- Low power consumption
- 8048-, 8085A-, and 8086-bus compatible
- 8-bit CPU with 2K × 8 ROM and 128 × 8 RAM
- 8-bit timer/counter
- 18 I/O lines
- 8-bit status register
- Two data registers for asynchronous slave-to-master interface
- Interrupt, DMA, or polled operation
- Expandable I/O
- Two power down modes
- 8041A-, 8741A-pin compatible
- On-chip clock generator
- Single +5 V power supply

Ordering Information

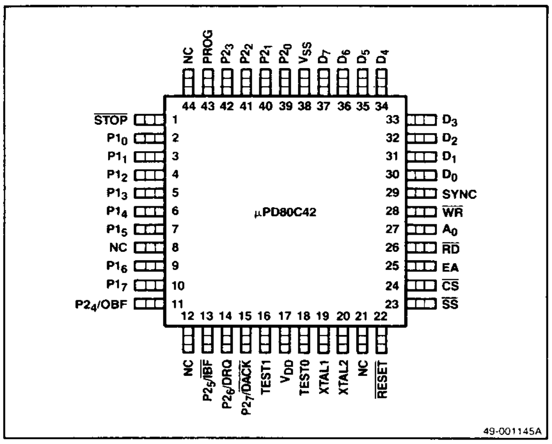
Part Number	Package Type	Max Frequency of Operation
μPD80C42C	40-pin plastic DIP	8 MHz
μPD80C42G-22	44-pin plastic miniflat	8 MHz

Pin Configurations

40-Pin Plastic DIP



44-Pin Plastic Miniflat



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Pin Identification

Plastic DIP

No.	Symbol	Function
1	TEST0	Test 0 input
2, 3	XTAL1, XTAL2	Crystal input
4	$\overline{\text{RESET}}$	Reset input
5	$\overline{\text{SS}}$	Single-step input
6	$\overline{\text{CS}}$	Chip select input
7	EA	External access input
8	$\overline{\text{RD}}$	Read input
9	A_0	Address input
10	$\overline{\text{WR}}$	Write input
11	SYNC	Synchronize output
12–19	D_0–D_7	Bidirectional port
20	V_{SS}	Ground
21–24	$P2_0$–$P2_3$	Quasi-bidirectional port 2
35–38	$P2_4$ / OBF, $P2_5$ / $\overline{\text{IBF}}$, $P2_6$ / DRQ, $P2_7$ / $\overline{\text{DACK}}$	Output buffer full, input buffer full, DMA request, DMA acknowledge
25	PROG	PROG output strobe
26	$\overline{\text{STOP}}$	$\overline{\text{STOP}}$ input
27–34	$P1_0$–$P1_7$	Quasi-bidirectional port 1
39	TEST1	Test 1 input
40	V_{DD}	Positive power supply
—	NC	No connection

Plastic Miniflat

No.	Symbol	Function
18	TEST0	Test 0 input
19, 20	XTAL1, XTAL2	Crystal input
22	$\overline{\text{RESET}}$	Reset input
23	$\overline{\text{SS}}$	Single-step input
24	$\overline{\text{CS}}$	Chip select input
25	EA	External access input
26	$\overline{\text{RD}}$	Read input
27	A_0	Address input
28	$\overline{\text{WR}}$	Write input
29	SYNC	Synchronize output
30–37	D_0–D_7	Bidirectional port
38	V_{SS}	Ground
39–42	$P2_0$–$P2_3$	Quasi-bidirectional port 2
11, 13–15	$P2_4$ / OBF, $P2_5$ / $\overline{\text{IBF}}$, $P2_6$ / DRQ, $P2_7$ / $\overline{\text{DACK}}$	Output buffer full, input buffer full, DMA request, DMA acknowledge
43	PROG	PROG output strobe
1	$\overline{\text{STOP}}$	$\overline{\text{STOP}}$ input
2–7, 9–10	$P1_0$–$P1_7$	Quasi-bidirectional port 1
16	TEST1	Test 1 input
17	V_{DD}	Positive power supply
8, 12, 21, 44	NC	No connection

Pin Functions

XTAL1, XTAL2 (Crystal)

XTAL1 and XTAL2 are the inputs for the crystal oscillator for the LC circuit generating internal clock signals. Use XTAL1 as the external clock input.

TEST0 (Test 0)

TEST0 is a testable input using conditional jump instructions JT0 and JNT0. TEST0 also resets the HALT mode.

TEST1 (Test 1)

TEST1 is a testable input using conditional jump instructions JT0 and JNT0. TEST1 is also an input to the event counter.

$\overline{\text{RESET}}$ (Reset)

$\overline{\text{RESET}}$ inputs a system reset, resets the HALT mode, and controls the STOP mode.

$\overline{\text{SS}}$ (Single-Step)

$\overline{\text{SS}}$ is an input used with SYNC to step the program through each instruction.

$\overline{\text{CS}}$ (Chip Select)

$\overline{\text{CS}}$ inputs the chip select signal. An active low enables the data bus.

EA (External Access)

EA is an input that inhibits internal program memory fetches. Use EA to check the ROM contents when debugging programs.

$\overline{\text{WR}}$ (Write)

$\overline{\text{WR}}$ is an input used by the master CPU to write data and commands into the data bus buffer in (DBBIN) register.

$\overline{\text{RD}}$ (Read)

$\overline{\text{RD}}$ is the input used by the master CPU to read data or status words from the data bus buffer out (DBBOUT) or status registers.

A_0 (Address 0)

A_0 is an address input that the master CPU uses to determine the bus operation as follows:

Cycle	A_0	Operation
Read	0	Data
	1	Status
Write	0	Data
	1	Command

SYNC (Synchronization)

SYNC is an output that occurs once per instruction cycle. SYNC is used as a strobe for external circuitry or to synchronize the single-step operation.

PROG (PROG output)

When using the I/O expansion port (μPD82C43), PROG outputs a strobe that outputs data/addresses $P2_0$–$P2_3$.

$\overline{\text{STOP}}$ (Stop)

The $\overline{\text{STOP}}$ input controls the hardware STOP mode.

D_0-D_7 (Port)

D_0-D_7 is a bidirectional port that transfers data between the data bus buffer (DBBOUT, DBBIN) registers and the 8-bit master CPU data bus.

$P1_0$-$P1_7$ (Port 1)

$P1_0$–$P1_7$ is a quasi-bidirectional, 8-bit port.

$P2_0$-$P2_7$ (Port 2)

$P2_0$–$P2_7$ is a quasi-bidirectional, programmable 8-bit port. $P2_4$–$P2_7$ (high-order bits) are alternative pins for the following interrupt request and DMA handshaking functions:

$P2_4$ = $\overline{\text{OBF}}$ (Output buffer full)
$P2_5$ = $\overline{\text{IBF}}$ (Input buffer full)
$P2_6$ = $\overline{\text{DRQ}}$ (DMA request)
$P2_7$ = $\overline{\text{DACK}}$ (DMA acknowledge)

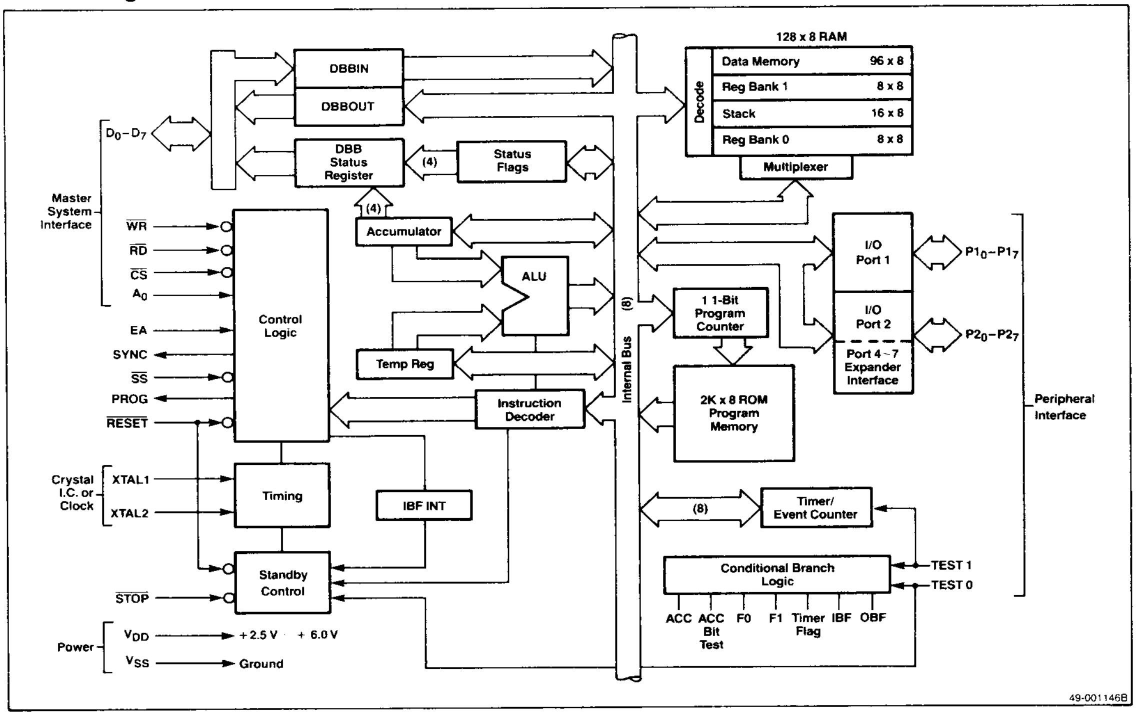
V_{DD} (Power Supply)

V_{DD} is the positive power supply (+2.5 V to +6.0 V)

V_{SS} (Ground)

V_{SS} is the ground potential.

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 V to +7 V
Input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Output voltage, V_O	−0.3 V to V_{DD} +0.3 V
Operating temperature, T_{OPT}	−40°C to +85°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Standard Voltage Range

$T_A = -40°C$ to $+85°C$, $V_{DD} = +5\,V \pm 10\%$, $V_{SS} = 0\,V$

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input voltage low	V_{IL}	−0.3		+0.8	V	
Input voltage high	V_{IH}	2.2		V_{DD}	V	Except $\overline{RESET}$, XTAL1, XTAL2
	V_{IH1}	$V_{DD}-1$		V_{DD}	V	$\overline{RESET}$, XTAL1, XTAL2
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 2.0\,mA$
Output voltage high	V_{OH}	2.4			V	D_0–D_7, SYNC, PROG; $I_{OH} = -400\,\mu A$
	V_{OH1}	2.4			V	Port 1, port 2; $I_{OH} = -50\,\mu A$
	V_{OH2}	$V_{DD}-0.5$			V	All outputs; $I_{OH} = -0.2\,\mu A$
Input current	I_{ILP}			−500	µA	Port 1, port 2; $V_I \leq V_{IL}$
	I_{ILC}			−40	µA	$\overline{SS}$, $\overline{RESET}$; $V_I \leq V_{IL}$
Input leakage current	I_{LI1}			±1	µA	T0, $\overline{T1}$, $\overline{STOP}$, $\overline{CS}$, A_0, $\overline{RD}$, $\overline{WR}$; $V_{SS} \leq V_I \leq V_{DD}$
	I_{LI2}			±3	µA	EA; $V_{SS} \leq V_I \leq V_{DD}$
Output leakage current	I_{LO}			±1	µA	$V_{SS} \leq V_O \leq V_{DD}$ High impedance, D_0–D_7, port
Standby current	I_{DD1}		1.5	3.0	mA	HALT mode; $t_{CY} = 1.25\,\mu s$
	I_{DD2}		2	20	µA	$\overline{STOP}$ mode (1)
Supply current	I_{DD}		10	20	mA	$t_{CY} = 1.25\,\mu s$
Data retention voltage	V_{DDDR}	2.0			V	STOP mode ($\overline{STOP}$, $\overline{RESET} \leq 0.4\,V$) or $\overline{RESET}$ ($\overline{RESET} \leq 0.4\,V$)

Note: (1) The input voltage pin is $V_I \leq V_{IL}$ or $V_I \geq V_{IH}$.

Extended Voltage Range

$T_A = -40°C$ to $+85°C$, $V_{DD} = +2.5\,V$ to $+6.0\,V$, $V_{SS} = 0\,V$

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input voltage low	V_{IL}	−0.3		+0.6	V	$2.5\,V \leq V_{DD} \leq 4.5\,V$
		−0.3		+0.8	V	$4.5\,V \leq V_{DD} \leq 6.0\,V$
Input voltage high	V_{IH}	$0.7V_{DD}$		V_{DD}	V	Except $\overline{RESET}$, XTAL1, XTAL2
	V_{IH1}	$0.8V_{DD}$		V_{DD}	V	$\overline{RESET}$, XTAL1, XTAL2
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 1.0\,mA$
Output voltage high	V_{OH}	$0.75V_{DD}$			V	D_0–D_7, SYNC, PROG; $I_{OH} = -100\,\mu A$
	V_{OH1}	$0.7V_{DD}$			V	Port 1, port 2; $I_{OH} = -10\,\mu A$
Input current	I_{ILP}			−500	µA	Port 1, port 2; $V_I \leq V_{IL}$
	I_{ILC}			−40	µA	$\overline{SS}$, $\overline{RESET}$; $V_I \leq V_{IL}$
Input leakage current	I_{LI1}			±1	µA	T0, $\overline{T1}$, $\overline{STOP}$, $\overline{CS}$, A_0, $\overline{RD}$, $\overline{WR}$; $V_{SS} \leq V_I \leq V_{DD}$
	I_{LI2}			±5	µA	EA; $V_{SS} \leq V_I \leq V_{DD}$
Output leakage current	I_{LO}			±1	µA	$V_{SS} \leq V_O \leq V_{DD}$ High impedance, D_0–D_7, port
Standby current	I_{DD1}		300	600	µA	HALT mode; $V_{DD} = 3\,V$; $t_{CY} = 5\,\mu s$
			2.0	4.0	mA	$V_{DD} = 6\,V$ $t_{CY} = 1.25\,\mu s$
	I_{DD2}		1	20	µA	STOP mode (1); $V_{DD} = 3\,V$
			2	50	mA	$V_{DD} = 6\,V$
Supply current	I_{DD}		2.0	5.5	mA	$V_{DD} = 3\,V$; $t_{CY} = 5\,\mu s$
			16	30	mA	$V_{DD} = 6\,V$; $t_{CY} = 1.25\,\mu s$
Data retention voltage	V_{DDDR}	2.0			V	STOP mode ($\overline{STOP}$, $\overline{RESET} \leq 0.4\,V$) or $\overline{RESET}$ ($\overline{RESET} \leq 0.4\,V$)

Note:
(1) The input voltage pin is $V_I \leq V_{IL}$ or $V_I \geq V_{IH}$.

AC Characteristics

Standard Voltage Range — DBB Read

$T_A = -0°C$ to $+70°C$, $V_{DD} = +5\,V \pm 10\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
$\overline{CS}$, A_0 setup to $\overline{RD}$ low	t_{AR}	0			ns	
$\overline{CS}$, A_0 hold from $\overline{RD}$ high	t_{RA}	0			ns	
$\overline{RD}$ pulse width	t_{RR}	200			ns	
$\overline{CS}$, A_0 to data output delay	t_{AD}			150	ns	$C_L = 100\,pF$
$\overline{RD}$ low to data output delay	t_{RD}			140	ns	$C_L = 100\,pF$
$\overline{RD}$ high to data float delay	t_{DF}	0		85	ns	
Cycle time	t_{CY}	1.25		15	μs	

Standard Voltage Range — DBB Write

$T_A = -0°C$ to $+70°C$, $V_{DD} = +5\,V \pm 10\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
$\overline{CS}$, A_0 setup to $\overline{WR}$ low	t_{AW}	0			ns	
$\overline{CS}$, A_0 hold from $\overline{WR}$ high	t_{WA}	0			ns	
$\overline{WR}$ pulse width	t_{WW}	200			ns	
data setup to $\overline{WR}$ high	t_{DW}	130			ns	
Data hold from $\overline{WR}$ high	t_{WD}	0			ns	

Extended Voltage Range — DBB Read

$T_A = -0°C$ to $+70°C$, $V_{DD} = +2.5\,V$ to $+6.0\,V$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
$\overline{CS}$, A_0 setup to $\overline{RD}$ low	t_{AR}	300			ns	
$\overline{CS}$, A_0 hold from $\overline{RD}$ high	t_{RA}	200			ns	
$\overline{RD}$ pulse width	t_{RR}	2000			ns	
$\overline{RD}$ low to data output delay	t_{RD}			1500	ns	$C_L = 100\,pF$
$\overline{RD}$ high to data float delay	t_{DF}	0		400	ns	
Cycle time	t_{CY}	5		15	μs	

Extended Voltage Range — DBB Write

$T_A = -0°C$ to $+70°C$, $V_{DD} = +2.5\,V$ to $6.0\,V$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
$\overline{CS}$, A_0 setup to $\overline{WR}$ low	t_{AW}	300			ns	
$\overline{CS}$, A_0 hold from $\overline{WR}$ high	t_{WA}	200			ns	
$\overline{WR}$ pulse width	t_{WW}	2000			ns	
data setup to $\overline{WR}$ high	t_{DW}	1500			ns	
Data hold from $\overline{WR}$ high	t_{WD}	200			ns	

Standard Voltage Range — Port 2

$V_{DD} = +5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Port control setup to PROG low	t_{CP}	100			ns	$C_L = 80\,pF$
Input port control hold from PROG low	t_{PC1}	0		80	ns	$C_L = 20\,pF$
Output port control hold from PROG low	t_{PC2}	135			ns	$C_L = 20\,pF$
Input data setup to PROG low	t_{PR}			650	ns	$C_L = 80\,pF$
Input data hold from PROG high	t_{PF}	0		150	ns	$C_L = 20\,pF$
Output data setup to PROG high	t_{DP}	200			ns	$C_L = 80\,pF$
Output data hold from PROG high	t_{PD}	60			ns	$C_L = 20\,pF$
PROG pulse width	t_{PP}	700			ns	

AC Characteristics (cont)

Extended Voltage Range — Port 2

V_{DD} = +2.5 V to +6.0 V

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Port control setup to PROG low	t_{CP}	460			ns	C_L = 80 pF
Input port control hold from PROG low	t_{PC1}	0		200	ns	C_L = 20 pF
Output port control hold from PROG low	t_{PC2}	1135			ns	C_L = 20 pF
Input data setup to PROG low	t_{PR}			2715	ns	C_L = 80 pF
Input data hold from PROG high	t_{PF}	0		500	ns	C_L = 20 pF
Output data setup to PROG high	t_{DP}	1850			ns	C_L = 80 pF
Output data hold from PROG high	t_{PD}	450			ns	C_L = 20 pF
PROG pulse width	t_{PP}	3250			ns	

Standard Voltage Range — DMA

V_{DD} = +5 V ± 10%

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
$\overline{\text{DACK}}$ setup to $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{ACC}	0			ns	
$\overline{\text{DACK}}$ hold from $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{CAC}	0			ns	
$\overline{\text{DACK}}$ to data output delay	t_{ACD}			140	ns	
$\overline{\text{RD}}$, $\overline{\text{WR}}$ to DRQ clear delay	t_{CRQ}			130	ns	C_L = 150 pF

Extended Voltage Range — DMA

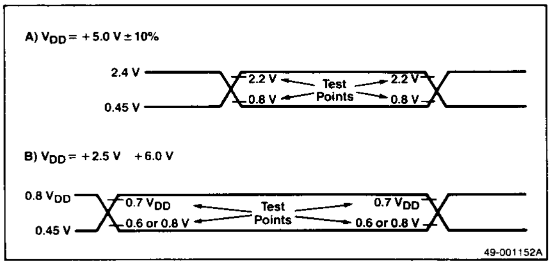
V_{DD} = +2.5 V to +6.0 V

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
$\overline{\text{DACK}}$ setup to $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{ACC}	200			ns	
$\overline{\text{DACK}}$ hold from $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{CAC}	200			ns	
$\overline{\text{DACK}}$ to data output delay	t_{ACD}			1500	ns	
$\overline{\text{RD}}$, $\overline{\text{WR}}$ to DRQ clear delay	t_{CRQ}			700	ns	C_L = 150 pF

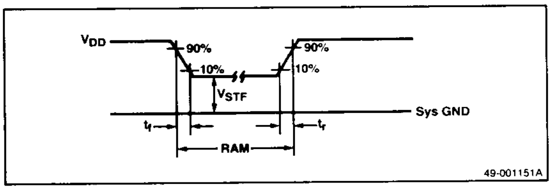
Standby Flag Retention Conditions

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Preservation of standby flag voltage fall time	t_f	100			μs	
Preservation of standby flag voltage rise time	t_r	100			μs	
Standby flag retention voltage	V_{STF}	2.0			V	

Input Waveforms for AC Test



Standby Flag Retention Timing

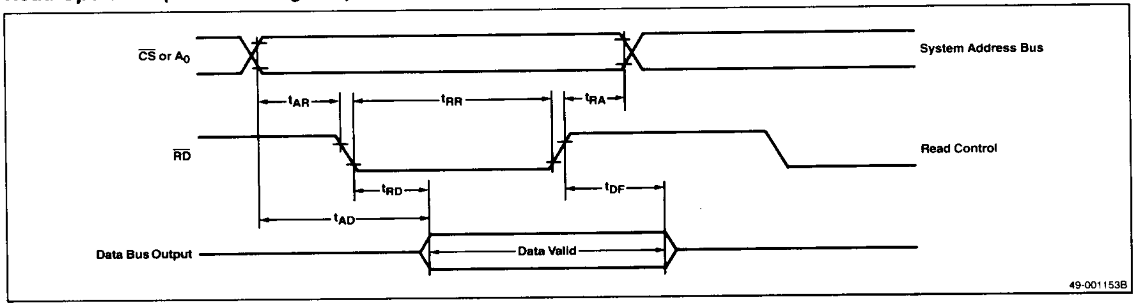


Bus Timing Requirements

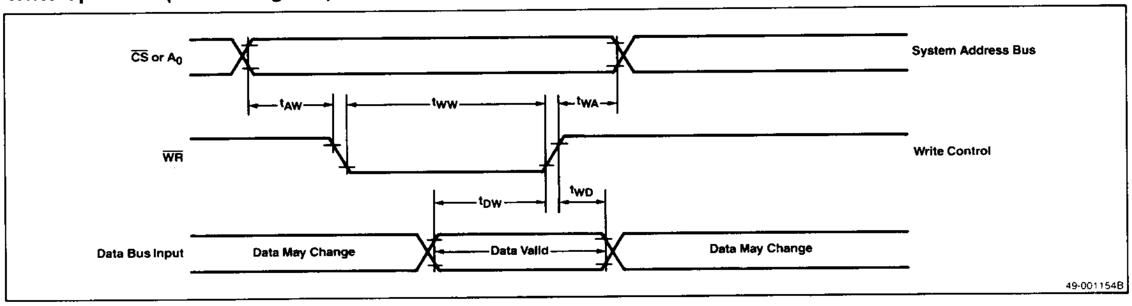
Symbol	Timing Formula	Min/Max	Unit
t_{CP}	$(1/10)\ t_{CY} - 40$	Min	ns
t_{PC2}	$(4/15)\ t_{CY} - 200$	Min	ns
t_{PR}	$(17/30)\ t_{CY} - 120$	Max	ns
t_{PF}	$(1/10)\ t_{CY}$	Max	ns
t_{DP}	$(2/5)\ t_{CY} - 150$	Min	ns
t_{PD}	$(1/10)\ t_{CY} - 50$	Min	ns
t_{PP}	$(7/10)\ t_{CY} - 250$	Min	ns
t_{CY}	$(1/f_{XTAL}) \times 15$		μs

Timing Waveforms

Read Operation (DBBOUT Register)



Write Operation (DBBIN Register)



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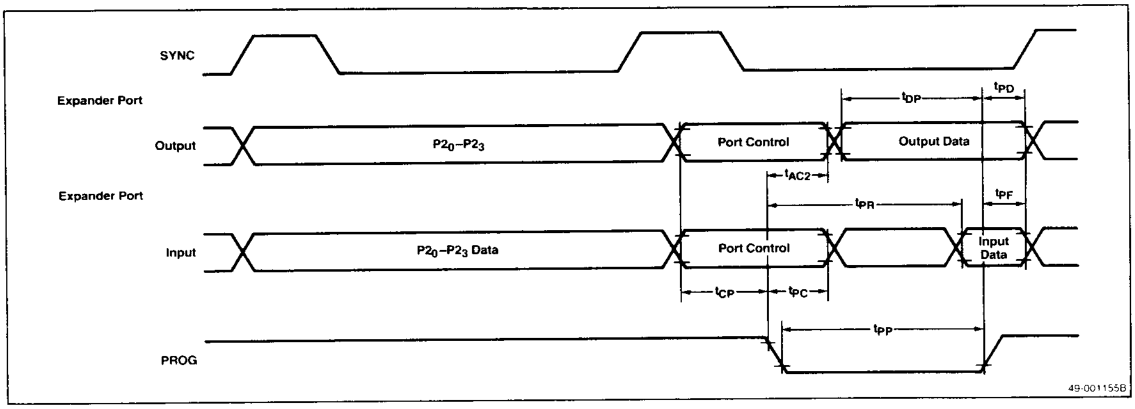
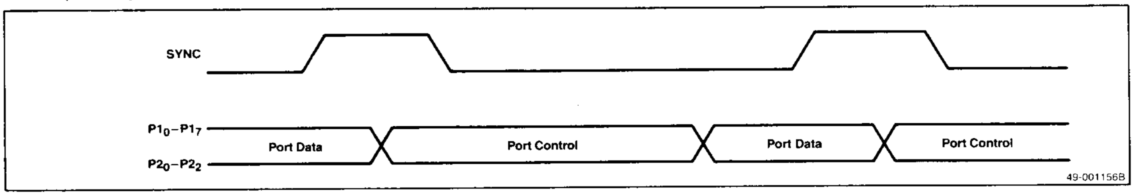
Timing Waveforms (cont)

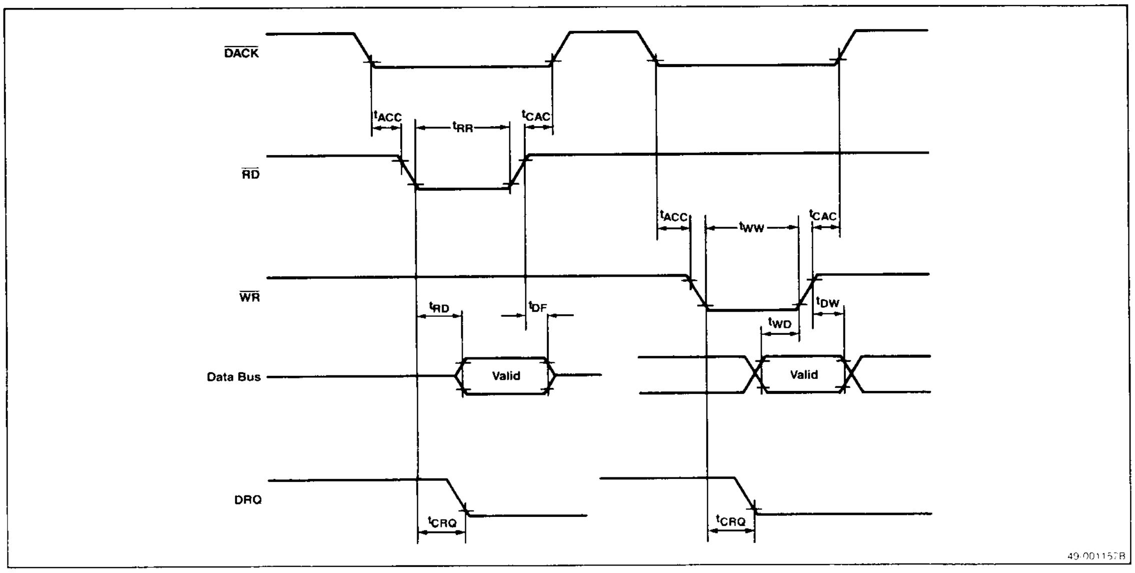
PORT2



PORT (EA = 1)



DMA

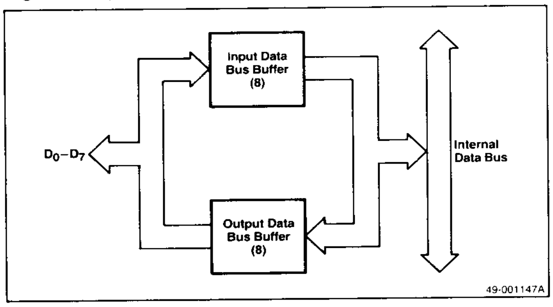


Functional Description

Data Bus Buffer In (DBBIN) and Data Bus Buffer Out (DBBOUT) Registers

As figure 1 shows, the DBBIN and DBBOUT registers transfer data to and from the master processors by way of the 8-bit external data bus (D_0–D_7) and the 8-bit internal data bus.

Figure 1. μPD80C42 Data Flow



Data Bus Buffer (DBB) Status Register

The μPD80C42 has an 8-bit status register (ST_0–ST_7) that contains information about the current status of the master or slave processor. The MOV STS, A instruction makes status bits ST_4–ST_7 user-definable by moving accumulator bits 4-1 to bits ST_4–ST_7 of the status register (ST_0–ST_3 are not affected). Bits ST_0–ST_3 give the status of the Output Buffer Full (OBF) and Input Buffer Full (IBF) bits, and flag bits (F0, F1). Figure 2 shows the status register format.

Figure 2. Status Register Format

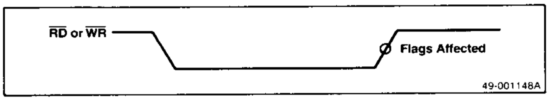
ST_7	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0
UD	UD	UD	UD	F1	F0	IBF	OBF

The MOV STS, A instruction is coded as follows:

1 0 0 1 0 0 0 0 90H

Figure 3 shows how ST_0–ST_3 change internally on the trailing-edge of $\overline{RD}$ or $\overline{WR}$ ($\overline{RD}$ and $\overline{WR}$ are edge-sensitive).

Figure 3. $\overline{RD}$ or $\overline{WR}$ Inputs



You can make ST_0 (OBF) and ST_1 (IBF) externally available in order to interrupt the master processor by executing the EN FLAGS instruction. When the EN FLAGS instruction is executed, $P2_4$ becomes the OBF pin. A 1 written to $P2_4$ enables OBF and outputs its status. A 0 written to $P2_4$ disables OBF by holding it low. Use OBF to indicate that valid data is available from the output data bus buffer register.

You can also use the EN FLAGS instruction to use $P2_5$ as the $\overline{IBF}$ pin. A 1 written to $P2_5$ enables $\overline{IBF}$ to output the inverse of the $\overline{IBF}$ status bit. A 0 written to $P2_5$ disables $\overline{IBF}$ by holding it low, making data at the data bus invalid.

The EN FLAGS instruction is coded as follows:

1 1 1 1 0 1 0 1 F5H

$P2_6$ and $P2_7$ are port pins or DMA handshake pins that allow a DMA interface. Use the EN DMA instruction to enable $P2_6$ and $P2_7$ as DRQ (DMA Request) and $\overline{DACK}$ (DMA Acknowledge), respectively. A 1 written to $P2_6$ activates DRQ, thus issuing a DMA request. Deactivate DRQ with the EN DMA instruction, $\overline{DACK}$ ANDed with $\overline{RD}$, or $\overline{DACK}$ ANDed with $\overline{WR}$. When EN DMA is executed, $P2_7$ ($\overline{DACK}$) functions as a chip select input for the data bus buffer registers during DMA transfers.

The EN DMA instruction is coded as follows:

1 1 1 0 0 1 0 1 E5H

HALT Mode

The HALT mode allows the μPD80C42 to conserve power during periods of inactivity. In the HALT mode, the oscillator remains active but the internal system clock stops. The HALT instruction allows the processor to enter the HALT mode.

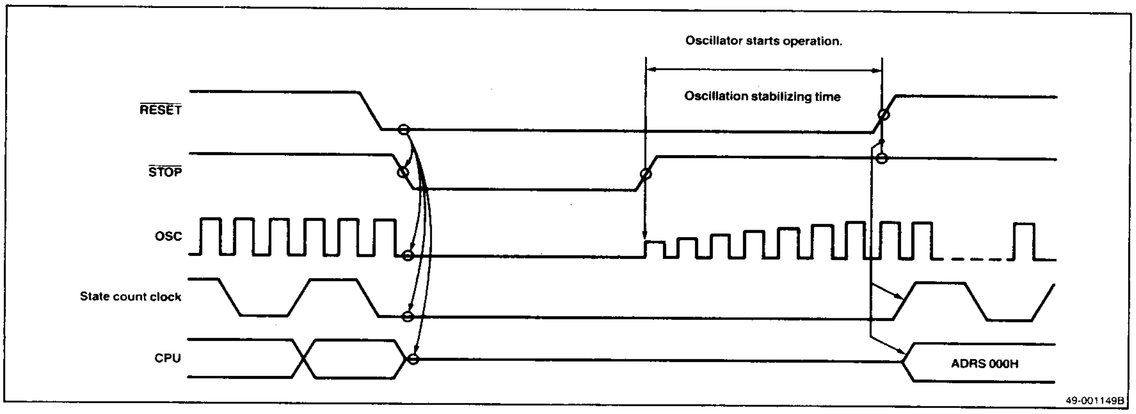
STOP Mode

The STOP mode disables the oscillator but maintains the contents of RAM. STOP mode conserves even more power than HALT mode. Enter STOP mode through software with the STOP instruction or through hardware with the $\overline{STOP}$ pin. In hardware STOP mode, the power supply voltage can drop as low as 2.0 V. In software STOP mode, it can drop as low as 2.5 V while still maintaining the RAM contents.

Control the STOP mode with hardware, with the $\overline{RESET}$ and $\overline{STOP}$ pins, as follows:

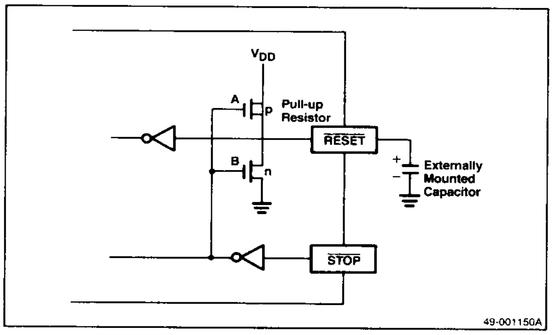
- Bring $\overline{RESET}$ low for at least six machine cycles, then bring $\overline{STOP}$ low. This assures proper termination of CPU operations. Figure 4 shows the timing for controlling STOP mode with hardware.

Figure 4. STOP Mode Control Timing



- Release hardware STOP mode by returning V_{CC} to +5 V ± 10%. After STOP goes high, hold RESET low long enough to allow the oscillator to stabilize. Figure 5 shows how to control oscillator settling time with the STOP pin by adding an external capacitor to the RESET line.
- Release the software STOP modes by applying a low level to the RESET pin to initiate oscillator operation. After sufficient oscillator stabilization time has passed, return RESET to a high level. Program execution will then begin at address 0.

Figure 5. STOP Mode Control Circuit



The following table shows the states of the output pins during both hardware and software STOP mode.

Table 1. Output Pins During STOP Mode

	State		
Output Pin	**STOPZ Instruction**	**STOPH Instruction**	**Hardware STOP**
$P1_0$–$P1_7$, $P2_0$–$P2_7$	High-Z	High level	High level
D_0–D_7	High-Z	High-Z	High-Z
PROG	High level	High level	High level
SYNC	Low level	Low level	Low level

Instruction Set

Mnemonic	Operation	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Accumulator												
ADD A, # data	(A), (C) ← (A) + data	Add immediate the specified data to the accumulator.(2)	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADD A, Rr	(A), (C) ← (A) + (Rr) r = 0–7	Add contents of designated register to the accumulator.(2)	0	1	1	0	1	r_2	r_1	r_0	1	1
ADD A, @ Rr	(A), (C) ← (A) + ((Rr)) r = 0–1	Add indirect the contents the data memory location to the accumulator.(2)	0	1	1	0	0	0	0	r_0	1	1
ADDC A, # data	(A), (C) ← (A) + (C) + data	Add immediate with carry the specified data to the accumulator.(2)	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADDC A, Rr	(A), (C) ← (A) + (C) + (Rr) r = 0–7	Add with carry the contents of the designated register to the accumulator.(2)	0	1	1	1	1	r_2	r_1	r_0	1	1
ADDC A, @ Rr	(A), (C) ← (A) + (C) + ((Rr)) r = 0–1	Add indirect with carry the contents of data memory location to the accumulator.(2)	0	1	1	1	0	0	0	r_0	1	1
ANL A, # data	(A) ← (A) AND data	Logical AND specified immediate data with accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ANL A, Rr	(A) ← (A) AND (Rr) r = 0–7	Logical AND contents of designated register with accumulator.	0	1	0	1	1	r_2	r_1	r_0	1	1
ANL A, @ Rr	(A) ← (A) AND ((Rr)) r = 0–1	Logical AND indirect the contents of data memory with accumulator.	0	1	0	1	0	0	0	r_0	1	1
CPL A	(A) ← NOT (A)	Complement the contents of the accumulator.	0	0	1	1	0	1	1	1	1	1
CLR A	(A) ← 0	Clear the contents of the accumulator.	0	0	1	0	0	1	1	1	1	1
DA A		Decimal adjust the contents of the accumulator.(2)	0	1	0	1	0	1	1	1	1	1
DEC A	(A) ← (A) − 1	Decrement by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ORL A, Rr	(A) ← (A) OR (Rr); r = 0–7	Logical OR contents of designated register with accumulator.	0	1	0	0	1	r_2	r_1	r_0	1	1
ORL A, @ Rr	(A) ← (A) OR ((Rr)) r = 0–1	Logical OR indirect the contents of data memory location with accumulator.	0	1	0	0	0	0	0	r_0	1	1
RL A	$(A_{n+1}) \leftarrow (A_n)$, $(A_0) \leftarrow (A_7)$ n = 0–6	Rotate accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1
RLC A	$(A_{n+1}) \leftarrow (A_n)$, $(A_0) \leftarrow (C)$ $(C) \leftarrow (A_7)$ n = 0–6	Rotate accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1
RR A	$(A_n) \leftarrow (A_{n+1})$, $(A_7) \leftarrow (A_0)$ n = 0–6	Rotate accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1

Instruction Set (cont)

Mnemonic	Operation	Description	Operation Code D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes
Accumulator (cont)												
RRC A	$(A_n) \leftarrow (A_{n+1})$, $(A_7) \leftarrow (C)$ $(C) \leftarrow (A_0)$ n = 0-6	Rotate accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1
SWAP A	$(A_7\text{–}A_4) \longleftrightarrow (A_3\text{–}A_0)$	Swap the 2 4-bit nibbles in the accumulator.	0	1	0	0	0	1	1	1	1	1
XRL A, # data	$(A) \leftarrow (A)$ XOR data	Logical XOR specified immediate data with accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
XRL A, Rr	$(A) \leftarrow (A)$ XOR (Rr) r = 0-7	Logical XOR contents of designated register with accumulator.	1	1	0	1	1	r_2	r_1	r_0	1	1
XRL A, @ Rr	$(A) \leftarrow (A)$ XOR ((Rr)) r = 0-1	Logical XOR indirect the contents of data memory location with accumulator.	1	1	0	1	0	0	0	r_0	1	1
Branch												
DJNZ Rr, addr	$(Rr) \leftarrow (Rr) - 1$; If $Rr \neq 0$: $(PC_7\text{–}PC_0) \leftarrow a_7\text{–}a_0$ r = 0-7	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r_2 a_2	r_1 a_1	r_0 a_0	2	2
JBb addr	$(PC_7\text{–}PC_0) \leftarrow a_7\text{–}a_0$ if Bb = 1 $(PC) \leftarrow (PC) + 2$ if Bb = 0	Jump to specified address if accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2
JC addr	$(PC_7\text{–}PC_0) \leftarrow a_7\text{–}a_0$ if C = 1 $(PC) \leftarrow (PC) + 2$ if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF0 addr	$(PC_7\text{–}PC_0) \leftarrow a_7\text{–}a_0$ if F0 = 1 $(PC) \leftarrow (PC) + 2$ if F0 = 0	Jump to specified address if flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF1 addr	$(PC_7\text{–}PC_0) \leftarrow a_7\text{–}a_0$ if F1 = 1 $(PC) \leftarrow (PC) + 2$ if F1 = 0	Jump to specified address if flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JMP addr	$(PC_{10}\text{–}PC_8) \leftarrow (a_7\text{–}a_0)$	Direct jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
JMPP @ A	$(PC_7\text{–}PC_0) \leftarrow ((A))$	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1
JNC addr	$(PC_7\text{–}PC_0) \leftarrow a_7\text{–}a_0$ if C = 0 $(PC) \leftarrow (PC) + 2$ if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNIBF addr	$(PC_7\text{–}PC_0) \leftarrow a_7\text{–}a_0$ if IBF = 0 $(PC) \leftarrow (PC) + 2$ if IBF = 1	Jump to specified address if interrupt is low.	1 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT0 addr	$(PC_7\text{–}PC_0) \leftarrow a_7\text{–}a_0$ if T0 = 0 $(PC) \leftarrow (PC) + 2$ if T0 = 1	Jump to specified address if test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT1 addr	$(PC_7\text{–}PC_0) \leftarrow a_7\text{–}a_0$ if T1 = 0 $(PC) \leftarrow (PC) + 2$ if T1 = 1	Jump to specified address if test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNZ addr	$(PC_7\text{–}PC_0) \leftarrow a_7\text{–}a_0$ if $A \neq 0$ $(PC) \leftarrow (PC) + 2$ if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2

Instruction Set (cont)

Mnemonic	Operation	Description	D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes
Branch (cont)												
JOBF addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if OBF = 1 $(PC) \leftarrow (PC) + 2$ if OBF = 0	Jump to specified address if output is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JTF addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if TF = 1 then reset TF $(PC) \leftarrow (PC) + 2$ if TF = 0	Jump to specified address if timer flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT0 addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jump to specified address if test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT1 addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if T1 = 1 $(PC) \leftarrow (PC) + 2$ if T1 = 0	Jump to specified address if test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JZ addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if A = 0 $(PC) \leftarrow (PC) + 2$ if A = 1	Jump to specified address if accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
Control												
EN I		Enable the interrupt.	0	0	0	0	0	1	0	1	1	1
DIS I		Disable the external interrupt input.	0	0	0	1	0	1	0	1	1	1
EN DMA		Enables DMA handshake lines.	1	1	1	0	0	1	0	1	1	1
EN Flags		Enables master interrupts.	1	1	1	1	0	1	0	1	1	1
SEL RB0	$(BS) \leftarrow 0$	Select bank 0 (locations 0–7) of data memory.	1	1	0	0	0	1	0	1	1	1
SEL RB1	$(BS) \leftarrow 1$	Select bank 1 (locations 24–31) of data memory.	1	1	0	1	0	1	0	1	1	1
HALT		Initiates halt mode.	0	0	0	0	0	0	0	1	1	1
STOP Z		Sets CPU to software stop mode. (Port output high impedance)	1	0	0	0	0	0	1	0	1	1
STOP H		Sets CPU to software stop mode. (Port output high level)	1	1	1	0	0	0	1	0	1	1
Data Moves												
MOV A, # data	$(A) \leftarrow$ data	Move immediate the specified data into the accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
MOV A, Rr	$(A) \leftarrow (Rr)$; r = 0–7	Move the contents of the designated registers into the accumulator.	1	1	1	1	1	r_2	r_1	r_0	1	1
MOV A, @ Rr	$(A) \leftarrow ((Rr))$; r = 0–1	Move indirect the contents of data memory location into the accumulator.	1	1	1	1	0	0	0	r_0	1	1
MOV A, PSW	$(A) \leftarrow (PSW)$	Move contents of the program status word into the accumulator.	1	1	0	0	0	1	1	1	1	1
MOV Rr, # data	$(Rr) \leftarrow$ data; r = 0–7	Move immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r_2 d_2	r_1 d_1	r_0 d_0	2	2
MOV Rr, A	$(Rr) \leftarrow (A)$; r = 0–7	Move accumulator contents into the designated register.	1	0	1	0	1	r_2	r_1	r_0	1	1
MOV @ Rr, A	$((Rr)) \leftarrow (A)$; r = 0–1	Move indirect accumulator contents into data memory location.	1	0	1	0	0	0	0	r_0	1	1
MOV @ Rr, # data	$((Rr)) \leftarrow$ data; r = 0–1	Move immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r_0 d_0	2	2
MOV PSW, A	$(PSW) \leftarrow (A)$	Move contents of accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1

Instruction Set (cont)

Mnemonic	Operation	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Data Moves (cont)												
MOVP A, @ A	A ← $((PC_{10}–PC_8), (A))$	Move data in the current page into the accumulator.	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	(A) ← ((011, A))	Move program data in page 3 into the accumulator.	1	1	1	0	0	0	1	1	2	1
XCH A, Rr	(A) ←→ (Rr); r = 0–7	Exchange the accumulator and designated register's contents.	0	0	1	0	1	r_2	r_1	r_0	1	1
XCH A, @ Rr	(A) ←→ ((Rr)); r = 0–1	Exchange indirect contents of accumulator and location in data memory.	0	0	1	0	0	0	0	r_0	1	1
XCHD A, @ Rr	$(A_3–A_0)$ ←→ $((Rr)_3–(Rr)_0)$; r = 0–1	Exchange indirect 4-bit contents of accumulator and data memory.	0	0	1	1	0	0	0	r_0	1	1
Flags												
CPL C	(C) ← NOT (C)	Complement contents of carry bit.	1	0	1	0	0	1	1	1	1	1
CPL F0	(F0) ← NOT (F0)	Complement contents of flag F0.	1	0	0	1	0	1	0	1	1	1
CPL F1	(F1) ← NOT (F1)	Complement contents of flag F1.	1	0	1	1	0	1	0	1	1	1
CLR C	(C) ← 0	Clear contents of carry bit to 0.	1	0	0	1	0	1	1	1	1	1
CLR F0	(F0) ← 0	Clear contents of flag 0 to 0.	1	0	0	0	0	1	0	1	1	1
CLR F1	(F1) ← 0	Clear contents of flag 1 to 0.	1	0	1	0	0	1	0	1	1	1
Input / Output												
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1–2	Logical AND immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p_1 d_1	p_0 d_0	2	2
ANLD Pp, A	(Pp) ← (Pp) AND $(A_3–A_0)$; p = 4–7	Logical AND contents of accumulator with designated port (4–7).	1	0	0	1	1	1	p_1	p_0	2	1
IN A, DBB	(A) ← (DBBIN); IBF ← 0		0	0	1	0	0	0	1	0	1	1
IN A, Pp	(A) ← (Pp); p = 1–2	Input data from designated port (1–2) into accumulator.	0	0	0	0	1	0	p_1	p_2	2	1
MOVD A, Pp	$(A_3–A_0)$ ← (Pp); $(A_7–A_4)$ ← 0 p = 4–7	Move contents of designated port (4–7) into accumulator.	0	0	0	0	1	1	p_1	p_0	2	1
MOVD Pp, A	(Pp) ← $(A_3–A_0)$; p = 4–7	Move contents of accumulator to designated port (4–7).	0	0	1	1	1	1	p_1	p_0	2	1
MOV STS, A	$(ST_7–ST_4)$ ← $(A_7–A_4)$	Move contents of accumulator to designated port (4–7).	1	0	0	1	0	0	0	0	1	1

Instruction Set (cont)

Mnemonic	Operation	Description	Operation Code D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes
Input / Output (cont)												
ORLD Pp, A	(Pp) ← (Pp) OR (A_3-A_0); p = 4-7	Logical OR contents of accumulator with designated port (4-7).	1	0	0	0	1	1	p_1	p_0	2	1
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1-2	Logical OR immediate specified data with designated port (1-2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p_1 d_1	p_0 d_0	2	2
OUT DBB, A	(DBBOUT) ← (A), OBF ← 1		0	0	0	0	0	0	1	0	1	1
OUTL Pp, A	(Pp) ← (A); p = 1-2	Output contents of accumulator to designated port (1-2).	0	0	1	1	1	0	p_1	p_0	2	1
Registers												
DEC Rr	(Rr) ← (Rr) − 1; r = 0-7	Decrement by 1 contents of designated register.	1	1	0	0	1	r_2	r_1	r_0	1	1
INC Rr	(Rr) ← (Rr) + 1; r = 0-7	Increment by 1 contents of designated register.	0	0	0	1	1	r_2	r_1	r_0	1	1
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0-1	Increment indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r_0	1	1
Subroutine												
CALL addr	((SP)) ← (PC), (PSW_7-PSW_4) (SP) ← (SP) + 1 (PC_{10}-PC_0) ← a_{10}-a_0	Call designated subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
RET	(SP) ← (SP) − 1 (PC) ← ((SP))	Return from subroutine without restoring program status word.	1	0	0	0	0	0	1	1	2	1
RETR	(SP) ← (SP) − 1 (PC) ← ((SP)) (PSW_7-PSW_4) ← ((SP))	Return from subroutine restoring program status word.	1	0	0	1	0	0	1	1	2	1
Timer / Counter												
EN TCNTI		Enable internal interrupt flag for timer / counter output.	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disable internal interrupt flag for timer / counter output.	0	0	1	1	0	1	0	1	1	1
MOV A, T	(A) ← (T)	Move contents of timer / counter into accumulator.	0	1	0	0	0	0	1	0	1	1
MOV T, A	(T) ← (A)	Move contents of accumulator into timer / counter.	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stop count for event counter.	0	1	1	0	0	1	0	1	1	1
STRT CNT		Start count for event counter.	0	1	0	0	0	1	0	1	1	1
STRT T		Start count for timer.	0	1	0	1	0	1	0	1	1	1
Miscellaneous												
NOP		No operation performed.	0	0	0	0	0	0	0	0	1	1

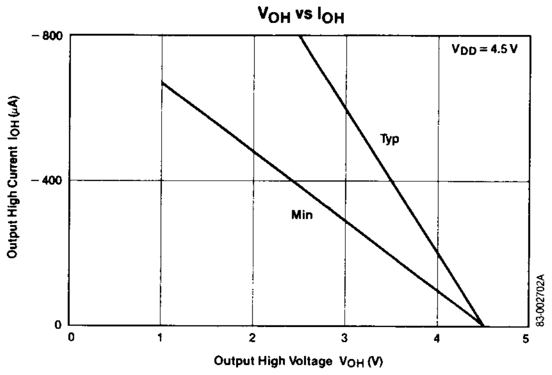
NEC

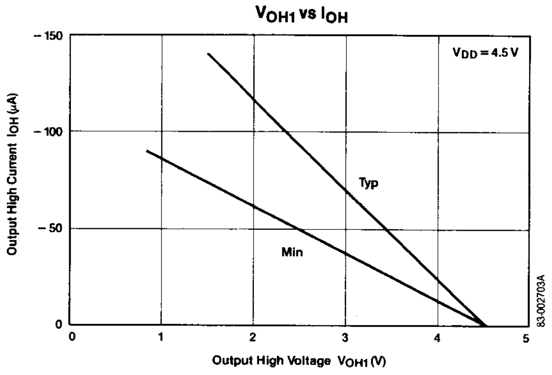
Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary carry flag
addr	Program memory address
b	Accumulator bit (b = 0–7)
C	Carry flag
CNT	Counter
data	8-bit data
DBB	Data bus buffer
F0, F1	Flags 0, 1 (C / D flag)
I	Interrupt
IBF	Input buffer full flag
OBF	Output buffer full flag
PC	Program counter
Pp	Port (p = 1–2 or 4–7)
PSW	Program status word
Rr	Register (r = 0–1 or r = 0–7)

Symbol	Description
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	TEST0, TEST1 pin
#	Immediate data
@	Indirect address
(x)	Contents of register X
((x))	Contents of memory addressed by X
←	Transfer direction, result
AND	Logical product (logical AND)
OR	Logical sum (logical OR)
XOR	Exclusive OR
———	Complement

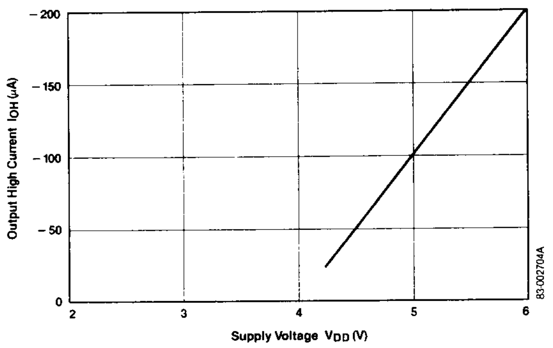
Operating Characteristics



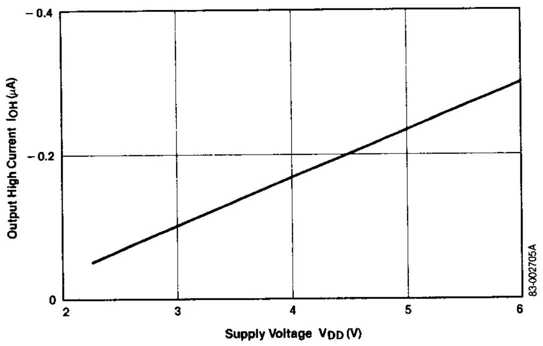


Operating Characteristics (cont)

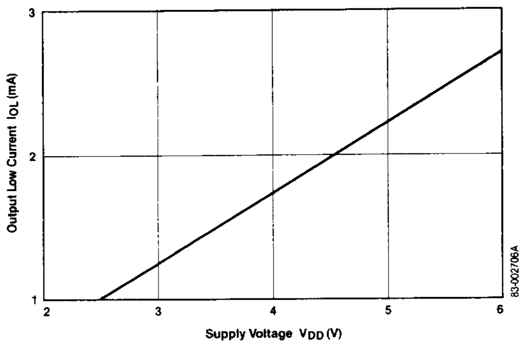
I_{OH} vs V_{DD} ($V_{OH1} = 2.4$ V)



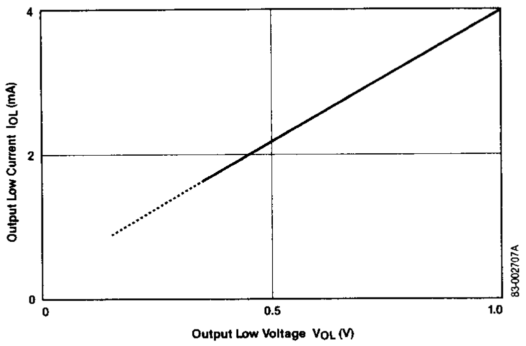
I_{OH} vs V_{DD} ($V_{OH2} = V_{DD} - 0.5$ V)



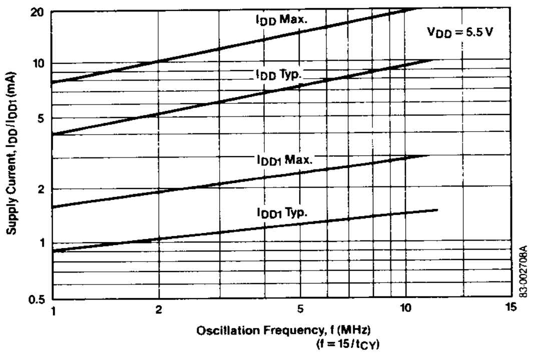
I_{OL} vs V_{DD} ($V_{OL} = 0.45$ V)



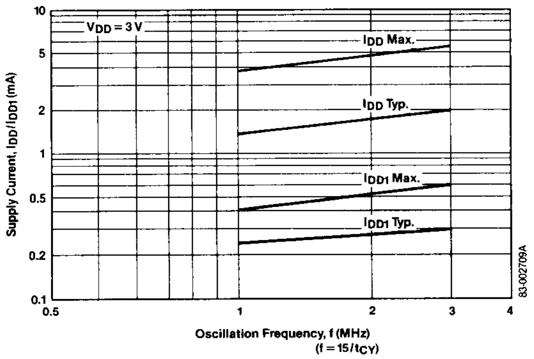
I_{OL} vs V_{DD} ($V_{DD} = 4.5$ V)



I_{DD}/I_{DD1} vs f($V_{DD} = 5.5$ V)



I_{DD}/I_{DD1} vs f($V_{DD} = 3$ V)



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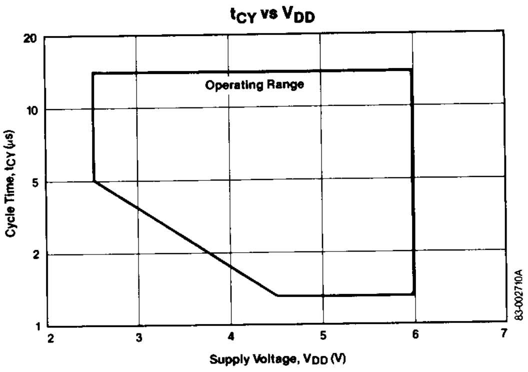
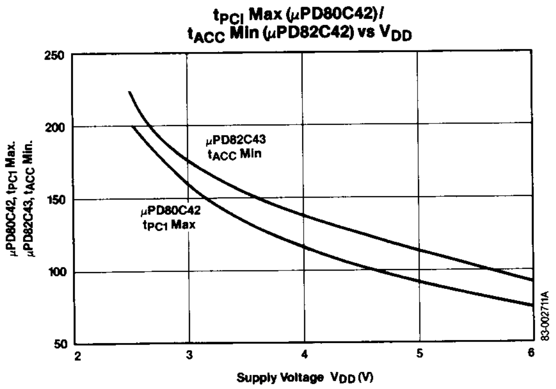
Operating Characteristics (cont)


t_{CY} vs V_{DD}
Operating Range
Cycle Time, t_{CY} (μs)
Supply Voltage, V_{DD} (V)
83-002710A


t_{PCI} Max (μPD80C42)/ t_{ACC} Min (μPD82C42) vs V_{DD}
μPD82C43 t_{ACC} Min
μPD80C42 t_{PC1} Max
μPD80C42, t_{PC1} Max. μPD82C43, t_{ACC} Min.
Supply Voltage V_{DD} (V)
83-002711A